REMARKS

The Applicants would like to thank the Examiner for the thorough examination of the present application. The arguments supporting patentability of the claimed invention are presented below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 12, 20 and 32 over the Smith patent in view of the Jain et al. patent. The Examiner also rejected independent Claim 27 over the Smith patent in view of the Jain et al. patent in further view of the Mejyr patent and the Matoba patent. Independent Claim 27 will also be discussed along with the rejection of independent Claims 12, 20 and 32.

The present invention, as recited in independent Claim 12, for example, is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each responsive to a respective local clock signal, and a system clock connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals. A power control manager is connected to the circuit blocks for selectively providing a shutdown signal thereto. Each circuit block comprises a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal to the power control manager.

An advantage of the present invention is that the shutdown circuit in each circuit block allows the circuit block to be safely shutdown after receiving the shutdown

signal. It can be difficult to establish an exact time when it is possible to switch off the clock to a circuit block without causing errors. In some cases, if the clock to the circuit block is stopped abruptly, there is a risk of preventing a critical operation of the circuit block from being carried out. For example, a circuit block could be performing a necessary communication protocol and the shutdown of the block could cause the SOC to disregard the protocol. Examples of protocols that could easily be disregarded include memory-DMA, and master-slave blocks among others. Additionally, removing a system clock from a counter or a timing signal generator could be fatal to that particular circuit block.

Independent Claim 20 is similar to independent Claim 12 except this claim recites a clock signal instead of a local clock signal, and each circuit block further comprises a block logic circuit having an input for receiving the shutdown signal and an output for providing the shutdown acknowledgement signal. Independent method Claim 32 is similar to independent device Claim 12.

Independent Claim 27 is similar to independent Claim 12 except this claim further recites that the power control manager is connected to the circuit blocks via a respective power down request line and a power down acknowledgement line, as well as reciting a central processing unit connected to the power control manager.

Referring now to Smith and to FIG. 1 in particular, the Examiner characterized the illustrated integrated circuit as a system-on-chip (SOC) comprising a plurality of circuit blocks **11-14**, a system clock connected to the circuit blocks

for providing a system clock signal **35** thereto, and a power control manager **1** connected to the circuit blocks for selectively providing a shutdown signal **15-18** thereto. The Examiner characterized each circuit block **11-14** as comprising a shutdown circuit (NAND gates **27-30** and **44-47**, flip-flops **23-26** and inverters **36-39**) for preventing the system clock signal **35** from functioning as the respective local clock signal based upon the shutdown signal.

The Examiner correctly acknowledges that Smith fails to provide a shutdown acknowledgement signal from anyone of the current blocks **11-14** to the power control manager **1** after having received the shutdown signal. The Examiner cited Jain et al. as disclosing this feature. FIG. 3 of Jain et al. discloses a clock synthesizer **304** having an active state and a clock stop state. The illustrated block diagram **300** implements C0, C1, C2 and C3 modes where C3 is a deep-sleep state. The Examiner references column 6, lines 6-23 which states that an acknowledgement signal of the C3 mode is issued. The Examiner has taken the position that it would have been obvious to modify Smith to include an acknowledgement signal as taught by Jain et al.

The Applicants respectfully submit that even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. With respect to Jain et al., the Examiner states that a power control manager is inherent and that a shutdown circuit is inherent. While this may appear to be the case, Jain et al. fails to clearly state that <u>each circuit block</u> comprises a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block

receiving the shutdown signal provides a shutdown acknowledgement signal to the power control manager. Reference is directed to the flowchart illustrated in FIG. 4 of Jain et al. in which the circuits are switched from the C0 mode (active power consumption) to the C3 mode (deep sleep state), and to column 4, lines 6-24, which provides:

> "FIG. 4 is a flowchart **400** illustrating one embodiment of a process for switching from a C0 mode to a C3 mode. A process begins at the start block and proceeds to block **402**. At block **402**, level three instructions are fetched and executed. After block **402**, the process proceeds to block **404**. At block **404**, the process halts CPU executions. After block **404**, the process proceeds to block **406** where the process allows CPU to enter C2 state. After block **406**, the process proceeds to block **408**. At block **408**, the process prepares the system to enter C3 mode. The preparation for the system to enter C3 state includes disabling AGP arbiters, claiming internal queues, flushing buffers, performing temperature and current calibration, broadcasting power down message, and the like. After block **408**, the process proceeds to block **410** where a signal of acknowledgement of C3 state is issued. After block **410**, the process proceeds to block **412**. At block **412**, processor clock is suspended and the C3 state is entered. After block **412** the process ends." (Emphasis added).

In particular, a power down message is broadcast when the C3 mode is to be entered, and an acknowledgement signal acknowledging that the C3 mode is ready to be entered is issued after the system has performed the necessary

preparations, i.e., disabling AGP arbiters, claiming internal queues, flushing buffers, performing temperature and current calibration, broadcasting power down message, and the like. The Applicants submit that the shutdown acknowledgement signal is also broadcast instead of being issued by the respective circuit blocks.

Moreover, the Applicants submit that Jain et al. fails to disclose that when each circuit block is to be powered down, each circuit block prevents the system clock signal from functioning as the respective local clock signal after receiving the shutdown signal and after providing a shutdown acknowledgement signal to the power control manager, as recited in independent Claim 12. The Applicants submit that since the power down message is broadcast when the C3 mode is to be entered, then the acknowledgement signal acknowledging that the C3 mode is ready to be entered is also broadcast. This is in sharp contrast to the claimed invention where each circuit block provides a shutdown acknowledgement signal after receiving the shutdown signal.

Therefore, the Applicants submit that independent Claim 12 is patentable over Smith in view of Jain et al. Independent Claims 20 and 32 are similar to independent Claim 12, and are also patentable over Smith in view of Jain et al.

The Mejyr patent and the Matoba patent were used in the rejection of independent Claim 27. The Examiner has taken the position that FIG. 1 in Mejyer discloses a power control manager **10** (i.e., processor A) provides a shutdown signal over a power down request line **11**, and receives a shutdown acknowledgment signal over a power down acknowledgement line **22**. The Examiner has taken the position that FIG. 1 in Matoba

discloses a power control manager **15** comprising at least one register **16a** indicating logic states of the shutdown signals. Matoba also discloses a central processing unit **CPU0** connected to the power control manager **15**. The Applicants submit that the Mejyr and Matoba patents fail to provide the deficiencies as discussed above with respect to Jain et al.

Therefore, the Applicants submit that independent Claim 27 is patentable over Smith in view of Jain et al. and in further view of the Mejyr and Matoba patents. In view of the patentability of independent Claims 12, 20, 27 and 32, their respective dependent claims, which recite yet further distinguishing features, are also patentable, and require no further discussion herein.

CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330

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